ISSUE 1

PROTOTYPING WITH AAL1GATOR-8 FOR AAL1GATOR-4 DESIGNS

PM73123-PM73124

AAL1GATOR-8 / AAL1GATOR-4

PROTOTYPING WITH AAL1GATOR-8 FOR AAL1GATOR-4 DESIGNS

APPLICATION NOTE

PROPRIETARY AND CONFIDENTIAL

ADVANCE

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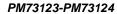
PM73123-PM73124

ISSUE 1

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ISSUE 1

PROTOTYPING WITH AAL1GATOR-8 FOR AAL1GATOR-4 DESIGNS

CONTENTS

1	INTRODUCTION	1
2	AAL1GATOR-8 / AAL1GATOR-4 BRIEF SUMMARY	2
3	HARDWARE CONSIDERATIONS	3
4	SOFTWARE CONSIDERATIONS	4
5	REFERENCES	5

ISSUE 1

PROTOTYPING WITH AAL1GATOR-8 FOR AAL1GATOR-4 DESIGNS

1 INTRODUCTION

The AAL1GATOR-8 device is scheduled to be available sooner than the AAL1GATOR-4. For those designs requiring the AAL1GATOR-4, it is possible to design schematics such that both the pin-compatible AAL1GATOR-8 and AAL1GATOR-4 can be populated in the same socket. What this allows is the use of the AAL1GATOR-8 for test and debugging purposes in the lab. For production boards, the AAL1GATOR-4, once available, can simply be populated in place of the AAL1GATOR-8.

To design a printed circuit board for the PM73123 AAL1GATOR-8 that is forward-compatible to the PM73124 (AAL1GATOR-4) requires a minimum of preparations. The preparations are divided into hardware considerations and software considerations.

This is a companion document to the followings:

- PMC-200-0082
 PM73123 AAL1GATOR-8 ATM Adaptation Layer 1 Segmentation and Reassembly Processor-8 Datasheet
- PMC-200-0083

 PM73124 AAL1GATOR-4 ATM Adaptation Layer 1 Segmentation and Reassembly Processor-4 Datasheet
- PMC-2000024- AAL1GATOR Product Family Technical Overview
- PMC-1991820
 AAL1GATOR Product Family Programmers Guide



ISSUE 1

PROTOTYPING WITH AAL1GATOR-8 FOR AAL1GATOR-4 DESIGNS

AAL1GATOR-8 / AAL1GATOR-4 BRIEF SUMMARY

The AAL1GATOR-8 provides circuit emulation of eight DS1/E1 links or a single DS3/E3 link. The AAL1GATOR-4 is a pin-compatible version of the AAL1GATOR-8 with support for four DS1/E1 links or a single DS3/E3 link. While AAL1GATOR-8 supports 256 VCs and 2 H-MVIP links, AAL1GATOR-4 supports 128 VCs and 1 H-MVIP link.

Both devices provide access to a 128k x 16 (18)- bit 10ns Synchronous SRAM or ZBT RAM and support a 52 MHz 16-bit UTOPIA L2 interface. For more information about the AAL1GATOR-8 and AAL1GATOR-4 devices, please refer to the documents listed in Section 5, References.

ISSUE 1

PROTOTYPING WITH AAL1GATOR-8 FOR AAL1GATOR-4 DESIGNS

3 HARDWARE CONSIDERATIONS

The following are the recommended hardware preparations:

- 1. Ground all package balls which are inputs that are present on the AAL1GATOR-8 but are not present on the AAL1GATOR-4:
 - RL_CLK(4-7), RL_SYNC(4-7), RL_DATA(4-7), RL_SIG(4-7), TL_SYNC(4-7).
 - TL_CLK(4-7) (If TL_CLK(0-3) are configured as inputs by TLCLK_OE asserted low.)
- 2. Leave unconnected all package balls which are outputs that are unused on the AAL1GATOR-8 but are not present on the AAL1GATOR-4:
 - TL_DATA(4-7), TL_SIG(4-7).
 - TL_CLK(4-7) (If TL_CLK(0-3) are configured as outputs by TLCLK_OE asserted high.)

APPLICATION NOTE PMC-2000095

ISSUE 1

PROTOTYPING WITH AAL1GATOR-8 FOR AAL1GATOR-4 DESIGNS

SOFTWARE CONSIDERATIONS

The following are the recommended software preparations.

- In the DEV_ID_REG normal mode register, for AAL1GATOR-8, DEV_TYPE=010, and for AAL1GATOR-4, DEV_TYPE=001.
- The JTAG ID Code is x3123 for the AAL1GATOR-8 and x3124 for the AAL1GATOR-4.
- AAL1GATOR-8 requires a different JTAG BSDL file than AAL1GATOR-4.

ISSUE 1

PROTOTYPING WITH AAL1GATOR-8 FOR AAL1GATOR-4 DESIGNS

REFERENCES 5

- 1. PMC-1991820- AAL1GATOR Product Family Programmers Guide
- PMC-2000024- AAL1GATOR Product Family Technical Overview 2.
- PMC-200-0082- PM73123 AAL1GATOR-8 ATM Adaptation Layer 1 3. Segmentation and Reassembly Processor-8 Datasheet
- PMC-200-0083- PM73124 AAL1GATOR-4 ATM Adaptation Layer 1 4. Segmentation and Reassembly Processor-4 Datasheet

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ISSUE 1

PROTOTYPING WITH AAL1GATOR-8 FOR AAL1GATOR-4 DESIGNS

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